CLAIMS

1. (original) An apparatus comprising:

a voltage converter to convert a voltage of a first value to an output voltage of a second value; and

a pulse frequency modulation unit to receive a feedback of the output voltage and to establish an upper limit level and lower limit level for the output voltage by use of a voltage mode control loop to maintain the output voltage from the converter near the second value determined by the upper and lower limit levels;

the pulse frequency modulation unit further including a filter to filter the feedback of the output voltage to detect sign changes at the filter when the upper and lower limit levels are detected and to skip a predetermined number of pulses from the filter after one of the sign changes to turn off the voltage converter.

2. (original) The apparatus of claim 1, wherein the pulse frequency modulation unit further includes a comparator in the feedback of the output voltage to compare the output voltage to a reference value to detect a sign change at a crossover point when upper and lower limit levels are reached by the output voltage, the sign change to be filtered and detected to generate the control signal.

3. (original) The apparatus of claim 2, wherein the voltage converter includes transistors which switch to generate the output voltage of the second value from a battery having a battery voltage of the first value, and wherein the control signal from the pulse frequency modulation unit controls operations of the transistors.

4. (original) The apparatus of claim 2, wherein the filter includes a high rate filter to filter high rate changes of the output voltage to provide a more rapid response to changes of the output voltage.

5. (original) A direct current to direct current (DC-DC) converter comprising:

a converter circuit to convert a battery voltage to an output voltage, the converter circuit including a pair of switching transistors that switch alternately to have the battery voltage converted to produce the output voltage; and

a control circuit to receive a feedback of the output voltage as part of a voltage mode control loop to maintain the output voltage within a specified value, the control circuit including an upper limit level detect circuit and a lower limit level detect circuit to detect upper and lower limit levels for the output voltage;

the control circuit to disable the converter circuit when the output voltage is at the upper limit level and to enable the converter circuit when the output voltage is at the lower limit level to maintain the output voltage between the upper and lower limit levels by use of the voltage mode control loop.

6. (original) The DC-DC converter of claim 5 wherein the control circuit further includes a comparator in the control loop to compare the output voltage to a reference value to detect a sign change at a crossover point, the sign change indicating when the output voltage has reached the upper or lower limit level and the sign change to be

detected by the upper and lower limit level detect circuits.

7. (original) The DC-DC converter of claim 6 further including a filter to receive an output from the comparator to detect the sign change to identify when the upper or lower limit level is reached.

8. (original) The DC-DC converter of claim 6 further including a high rate filter and a low rate filter to filter the output from the comparator to control switching operation of the pair of switching transistors, but only the high rate filter is used to generate a control signal to enable and disable the pair of transistors.

9. (original) The DC-DC converter of claim 7, wherein when the control circuit detects the upper or lower limit levels reached by the output voltage, the control circuit to skip a predetermined number of pulses from the filter after a sign change to ensure a steady state condition is substantially reached prior to initiating the control signal.

10. (original) The DC-DC converter of claim 9, wherein the control circuit further includes a pulse width modulation unit to receive a filtered output from the filter and generate pulse width modulated drive signals to control switching operation of the pair of transistors.

11. (original) An integrated circuit which has an audio system integrated therein, comprising:

an input interface to receive audio data input;

a digital signal processor to receive the audio input and generate processed audio data;

an output amplifier to output the processed audio data external to the integrated circuit; and

direct current to direct current (DC-DC) converter to power the digital signal processor and output amplifier by converting a battery voltage comprising:

a converter circuit to convert the battery voltage to an output voltage, the converter circuit including a pair of switching transistors that switch alternately to have the battery voltage converted to produce the output voltage; and

a control circuit to receive a feedback of the output voltage as part of a voltage mode control loop of the output voltage to maintain the output voltage within a specified value, the control circuit including an upper limit level detect circuit and a lower limit level detect circuit to detect upper and lower limit levels for the output voltage;

the control circuit to disable the converter circuit when the output voltage is at the upper limit level and to enable the converter circuit when the output voltage is at the lower limit level to maintain the output voltage between the upper and lower limit levels by use of the voltage mode control loop.

12. (original) The integrated circuit of claim 11, wherein the control circuit of the DC-DC converter further includes a comparator in the control loop to compare the output voltage to a reference value to detect a sign change at a crossover point, the sign change indicating when the output voltage has reached the upper or lower limit levels and the

sign change to be detected by the upper and lower limit level detect circuits.

13. (original) The integrated circuit of claim 12, wherein the DC-DC converter further including a high rate filter and a low rate filter to filter the output from the comparator to control switching operation of the pair of switching transistors, but only the high rate filter is used to generate a control signal to enable and disable the pair of transistors.

14. (original) The integrated circuit of claim 13, wherein when the control circuit detects the upper or lower limit levels reached by the output voltage, the control circuit to skip a predetermined number of pulses from the filter after a sign change to ensure a steady state condition is substantially reached prior to initiating the control signal.

15. (original) The integrated circuit of claim 14, wherein the control circuit further includes a pulse width modulation unit to receive a filtered output from the filter and generate pulse width modulated drive signals to control switching operation of the pair of transistors.

16. (original) The integrated circuit of claim 14, wherein the comparator includes a tapped voltage divider network at its input to divide the output voltage, in which a first tap point is used to select the lower limit level and a second tap point is used to select the upper limit level, the control circuit to control selection of the tap point in response to sign changes detected by the upper limit

level detect circuit and the lower limit level detect circuit.

17. (original) A method to provide voltage mode control loop in a direct current to direct current (DC-DC) converter comprising:

converting a battery voltage to an output voltage by using a DC-DC converter to have the battery voltage converted to produce the output voltage;

providing feedback of the output voltage to establish a voltage mode control loop to maintain the output voltage within a specified value between an upper limit level and a lower limit level; and

detecting the upper limit level and the lower limit level from the control loop to disable the DC-DC converter when the upper limit level is reached and to enable the converter when the lower limit level is reached.

18. (original) The method of claim 17, wherein the detecting the upper limit and lower limit levels includes comparing the output voltage to a reference value to detect a sign change at a crossover point, the sign change indicating when the output voltage has reached the upper or lower limit levels.

19. (original) The method of claim 18 further includes filtering to detect the sign change when one of the limit levels is reached to generate a control signal to enable and disable the pair of transistors.

20. (original) The method of claim 19, further including skipping a predetermined number of pulses from the

filtering after a sign change to ensure a steady state condition is substantially reached prior to initiating the control signal.